REMARKS

Claims 2, 6, 17-19 and 21-30 are pending in this application. By this Amendment, claims 21 and 24 are amended to further clarify that each of the comparators serves one row only, and claim 26 is amended to correct an informality. No new matter is added by this Amendment.

The courtesies extended to Applicant's representative by Examiner Hu at the interview held February 14, are appreciated. The reasons presented at the interview as warranting favorable action are incorporated into the remarks below and constitute Applicant's record of the interview.

I. Claim Objections

Claims 2, 6, 17-19 and 21-30 are objected to because in claim 1 "one for each row" needs to be further clarified as to whether each of the recited comparators is only for one row or for each row; and claim 24 "provided corresponding" needs to be further clarified to show in which way the recited comparators correspond with the recited electrodes; and in claim 26 "their electrode" should read "third electrode."

Claim 21 is amended to clarify that each of the comparators serves only one row. Claim 24 has been similarly amended. Claim 4 has been further amended to further clarify the overall configuration. Claim 6 is amended as suggested by the Examiner.

Accordingly, the requirements of the Patent Office are met. Withdrawal of the objections is respectfully requested.

II. Claim Rejections Under 35 U.S.C. §102(b) and §103(a)

Claims 2, 21, 22 and 24-28 are rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 3,599,185 (Bartlett); and claims 6, 17-19, 23, 29 and 30 are rejected under 35 U.S.C. §103(a) over Bartlett in view of JP 04-38866 (Adachi). These rejections are respectfully traversed.

The Office Action cites Figs. 4 and 5 of Bartlett and alleges that Bartlett discloses comparators, each for a row of the memory array that can naturally function to compare the first voltage from the first layer and the second voltage from the second layer through first and second inputs connected respectively to the first and third electrodes, so as to register a storage signal. However, this is not a disclosure of the comparator, as recited in independent claims 21 and 24, and as illustrated at, for example, Fig. 4 of the present application.

Bartlett discloses a memory device 10 that is written to and read from. See Fig. 1 of Bartlett. Bartlett further discloses that binary information is stored in the memory device. First, piezoelectric layer 14 is polarized by the application, via switches S1 and S2, of a positive voltage (Vp) to electrode 20 and a ground potential to electrode 18. Then a binary "1" is stored in the ferroelectric layer 12 by the application, via switches S3 and S2, of a positive potential (+ Vp) to electrode 16 and ground potential to electrode 20. Conversely, a binary "0" is stored in the ferroelectric layer by the application of a ground potential to electrode 16 and a positive potential (+Vp) to electrode 20. See col. 2, line 56 to col. 4, line 11 of Bartlett.

To read the binary state of the memory device, the switches S1, S2 and S3 are configured in the state as shown in Fig. 1 (see col. 4, lines 11-37 of Bartlett). During this reading operation, an interrogating pulse Vin is applied to electrode 18, while electrode 20 is at ground potential. This pulse creates a change in the physical dimensions of the piezoelectric layer 14, which likewise creates a change in the physical dimensions of the ferroelectric layer 12. This latter change causes a voltage to appear across the electrodes 16 and 20. This voltage on the "OUT" line is shown as voltage Vo on electrode 16 relative to a ground potential on electrode 20. This implies that Vo is read *relative to the ground potential* (as disclosed in Bartlett) *and not relative to the potential on electrode 18*, as recited in claims 21 and 24.

Furthermore, Fig. 4 of Bartlett is a detailed representation of each of the amplifiers A1 and A2 shown in Fig. 2 of Bartlett. Amplifiers A1, A2 amplify the signals on the upper electrode 12 of the memory devices. In Fig. 4 of Bartlett, these signals are taken along lines BL-1, BL-2 to respective amplifiers A1, A2. The signal on BL-1, BL-2 is fed to one input of a differential amplifier stage DA, while the other input thereof is fed with a reference potential V_R. Accordingly, the signal on lines BL-1, BL-2 (i.e., the signal on electrode 16) *is compared with the reference potential, V_R, not with any signal on electrode 18 via lines DL-1, DL-2.*

Moreover, Fig. 5 of Bartlett is a detailed representation of the register circuit SR shown in Fig. 2 of Bartlett. In this circuit, a comparison is made purely between output signals S and R of the amplifier circuit of Fig. 4 of Bartlett. The relative levels of these signals causes transistors 258 and 260 to output either a "1" or a "0", as shown. This does not suggest any kind of comparison with a signal on the electrode 18.

Thus, according to Bartlett, there is no direct comparison between the signals on electrodes 16 and 18, as recited in claims 21 and 24.

Adachi fails to cure the deficiencies discussed above with respect to Bartlett.

For the foregoing reasons, Bartlett, whether alone or taken with Adachi, fail to disclose or suggest the features of claims 21 and 24, as well as the claims depending therefrom.

III. Conclusion

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of the pending claims are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

Linda M. Saltiel
Registration No. 51,122

JAO:LMS/eks

Attachment:
Request for Continued Examination

Date: March 15, 2006

OLIFF & BERRIDGE, PLC
P.O. Box 19928
Alexandria, Virginia 22320
Telephone: (703) 836-6400

DEPOSIT ACCOUNT USE AUTHORIZATION
Please grant any extension necessary for entry;
Charge any fee due to our Deposit Account No. 15-0461